AMENDMENTS TO THE CLAIMS

Please find below a complete listing of the claims in the application, including their status as effected by the present amendment:

1) (*cancelled*)

2) (*cancelled*)

3) (*cancelled*)

4) (*cancelled*)

5) (*currently amended*) A router [[~~as defined in claim 4~~]], comprising:

a) a routing layer, said routing layer including a plurality of I/O ports for exchanging data with components external to said router;

b) a switching layer to switch data packets between I/O ports of said routing layer, said switching layer including an array of cells in communication with said routing layer for permitting exchange of data packets between said array of cells and said routing layer;

c) each cell including a memory for receiving a data packet from said routing layer;

d) said routing layer including a controller to control release of a data packet toward a cell of said array at least in part on a basis of a degree of occupancy of the memory in said cell;

wherein said routing layer further includes a memory for storing data packets for release to said switching layer, said controller controlling release of data packets from the memory of said routing layer;

wherein the memory of said routing layer includes an area for storing data indicative of a degree of occupancy of the memory of said cell;

wherein said controller is in communication with said memory to obtain access to the data indicative of a degree of occupancy of the memory of said

cell, said controller controlling release of data packets from the memory of said routing layer at least in part on a basis of the data indicative of a degree of occupancy of the memory of said cell;

wherein the memory of said routing layer includes a plurality of areas associated with respective cells of said array, each area operative to store data indicative of a degree of occupancy of the memory of a corresponding cell.

6) (*original*) A router as defined in claim 5, wherein said controller is responsive to a control signal issued by said switching layer to alter the data indicative of a degree of occupancy of the memory of a given cell in the area associated with the given cell.

7) (*original*) A router as defined in claim 6, wherein each cell of said switching layer is operative to issue a control signal to said controller to convey to said controller data indicative of the degree of occupancy of the memory of the cell.

8) (*original*) A router as defined in claim 7, wherein the memory of each cell is partitioned into slots, each slot capable of storing a data packet.

9) (*original*) A router as defined in claim 8, wherein each area associated with a given cell of said array is partitioned into zones, each zone being associated with a slot of the memory of the given cell, each zone containing data indicating if the associated slot of the memory of the given cell is available for reception of a data packet.

10) (*original*) A router as defined in claim 9, wherein each cell of said array, in response to release of a data packet from a certain slot of the memory of the cell, issues the control signal to convey to said controller data indicative of the degree of occupancy of the memory of the cell.

11) (*original*) A router as defined in claim 10, wherein the control signal contains information identifying the certain slot of the memory of the cell.

12) (*original*) A router as defined in claim 11, wherein said controller is responsive to the control signal containing information identifying the certain slot of the memory of the cell to alter the data in the zone of the memory of the routing layer associated with the certain slot.

13) (*cancelled*)

14) (*currently amended*) A switch fabric [[~~as defined in claim 13,~~]] implemented on a chip, comprising:

a) an array of cells;

b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) each cell communicating with at least one other cell of said array permitting exchange of data packets between the cells of said array;

d) each cell including:

I) a memory for receiving a data packet from said I/O interface; and

II) a control signal path for transporting a control signal to a component external to said array of cells, the control signal being indicative of a degree of occupancy of said memory;

wherein said memory is partitioned into slots, each slot capable of storing a data packet.

15) (*currently amended*) A switch fabric [[~~as defined in claim 14,~~]] implemented on a chip, comprising:

a) an array of cells;

b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) each cell communicating with at least one other cell of said array permitting exchange of data packets between the cells of said array;

d) each cell including:

I) a memory for receiving a data packet from said I/O interface; and

II) a control signal path for transporting a control signal to a component external to said array of cells, the control signal being indicative of a degree of occupancy of said memory;

wherein said memory is partitioned into slots, each slot capable of storing a data packet;

wherein the control signal indicative of a degree of occupancy of said memory contains information indicating whether a slot of said memory is free to accept a data packet.

16) (*previously presented*) A switch fabric as defined in claim 15, wherein in response to release of a data packet from a certain slot of said memory, said cell generating the control signal, the control signal including information identifying the certain slot.

17) (*cancelled*)

18) (, ' *cancelled*)

19) (*new*) A switch fabric as defined in claim 14, wherein in response to release of a data packet from a certain slot of said memory, said cell generating the control signal, the control signal including information identifying the certain slot.